4

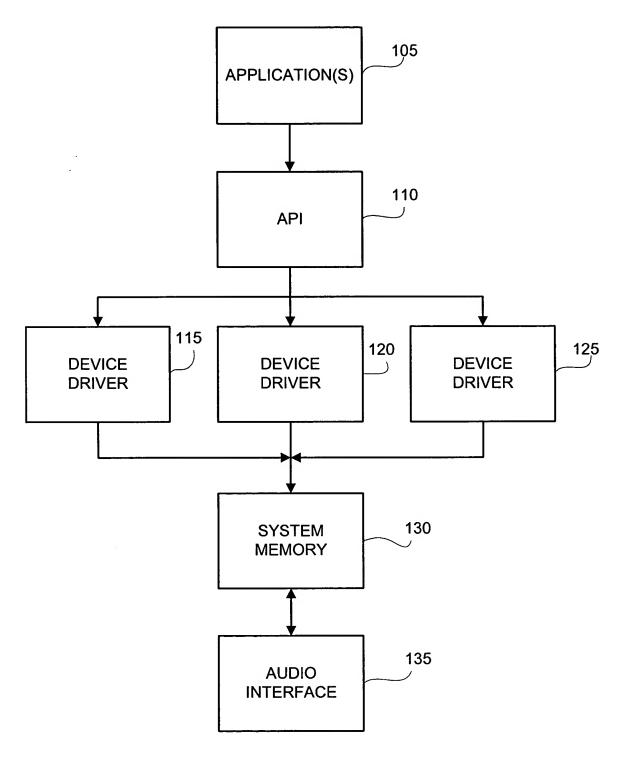


FIG. 1

+



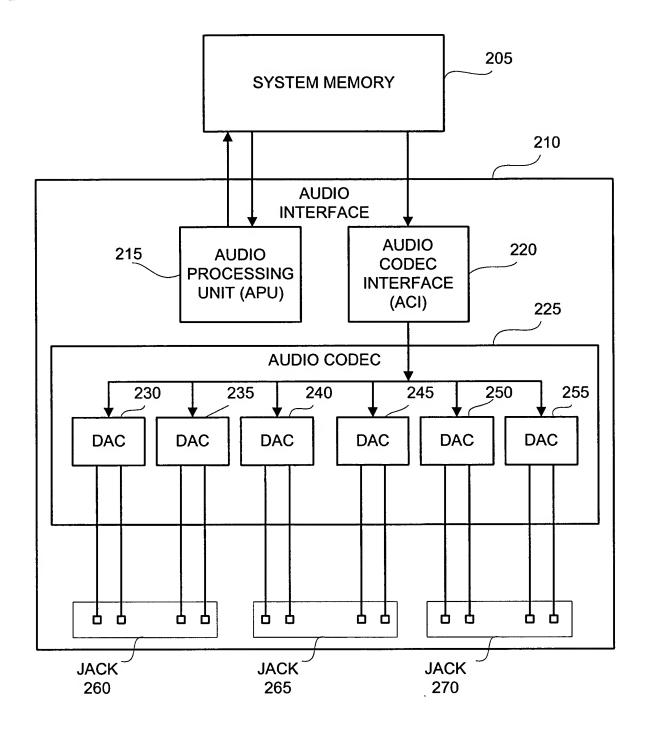


FIG. 2

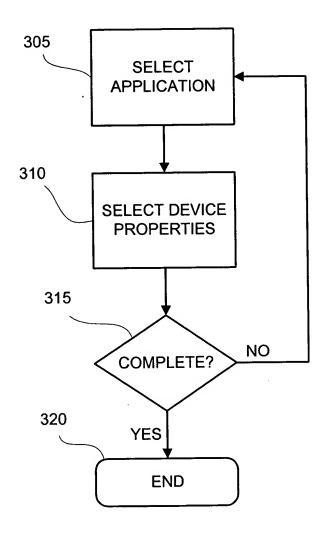


FIG. 3

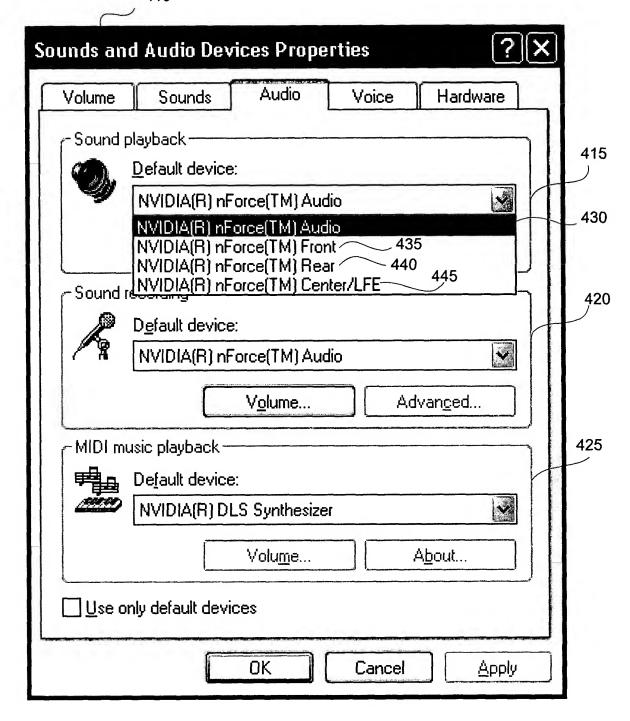


FIG. 4

+

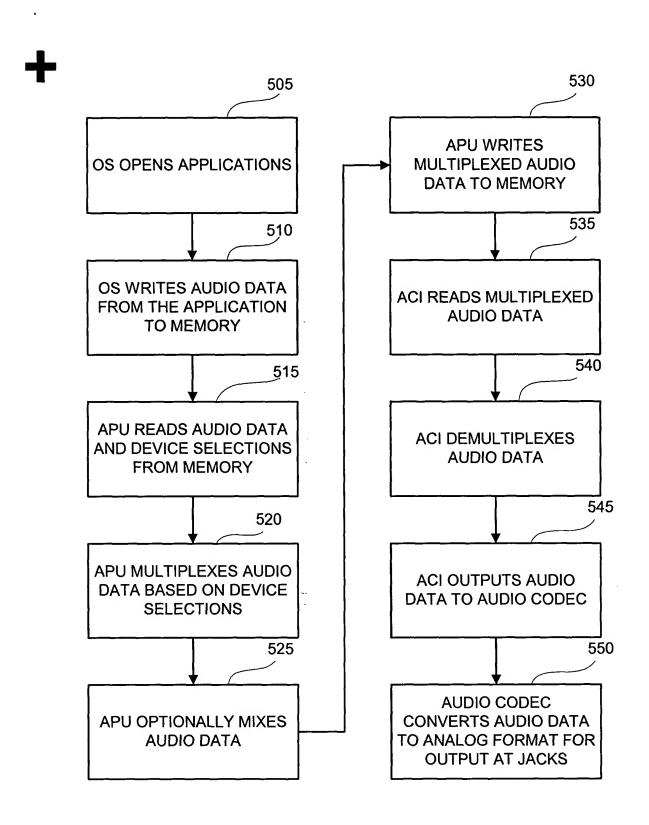


FIG. 5



АРР	DATA	CHANNEL
1	AB/CD/	01
2	EF/GH/	45
3	IJ/KĽ	23

FIG. 6A

APU 215 OUTPUT	A B I J E F / C D K L G H
DEVICE SEQUENCE	0 1 2 3 4 5 / 0 1 2 3 4 5

FIG. 6B



DATA INPUT 1	DATA INPUT 2	ОИТРИТ
AB/CD/	EF/GH/	ZY/VW/

FIG. 7